RISC-V: AN EXPLOSION IN AI ACCELERATORS FOR HPC

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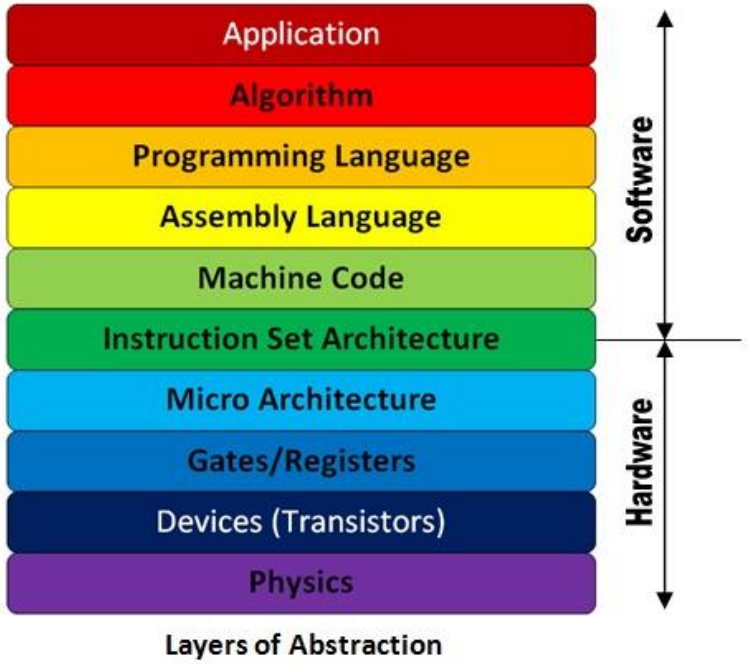
What is RISC-V?

- An open Instruction Set Architecture (ISA) which is overseen by RISC-V International
  - Standardisation activities driven by expert members
  - Numerous areas of focus ranging from HPC & ML to the data centre to embedded computing
- Why is this interesting for HPC?
  - Can freely develop new technologies based upon RISC-V
  - As the standards are community driven then we can shape this to suite our needs
  - Modula design of ISA means can pick and mix the parts that you need (ranging from low power embedded devices to HPC and AI accelerators)

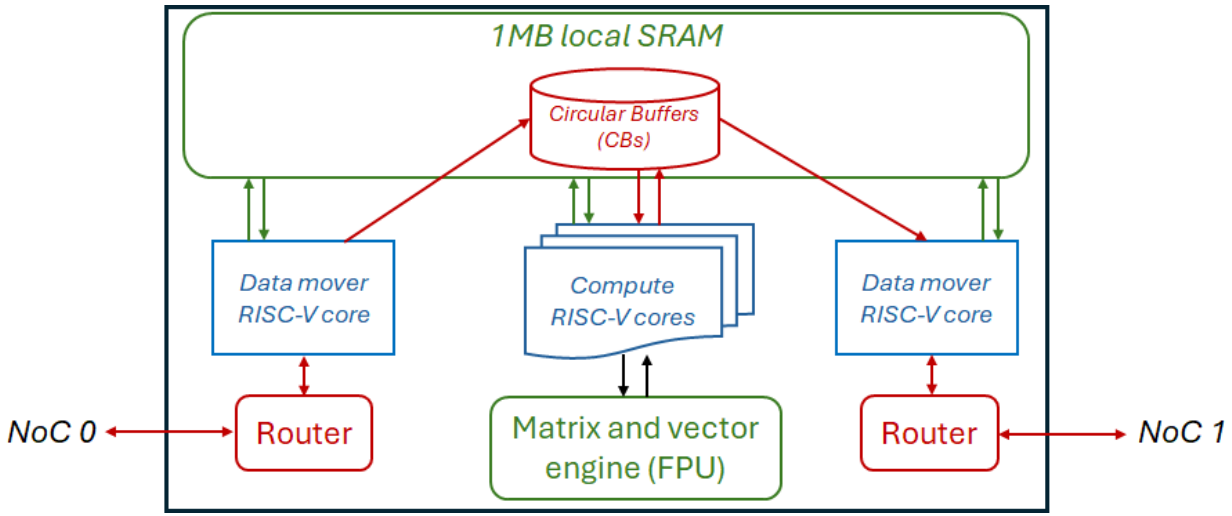


- Phenomenal growth
  - Qualcomm has shipped over a billion devices built upon RISC-V
  - Between 10 and 40 RISC-V cores in every Nvidia GPU
  - Over 16-billion RISC-V devices shipped by 2024

4U Server with 8 Thunderbird cards

Jacobi iteration on Grayskull e150

- Explored Jacobi iteration solving LaPlace's equation for diffusion on the Tenstorrent Grayskull



Type	Total cores	Cores in Y	Cores in X	Performance (GPt/s)	Energy (Joules)
CPU	1	-	-	1.41	1657
CPU	24	-	-	21.61	588
e150	1	1	1	1.06	2094
e150	2	1	2	2.48	893
e150	4	1	4	2.92	744
e150	8	4	4	7.99	276
e150	32	8	4	9.20	240
e150	64	8	8	12.96	170
e150	72	8	9	17.26	128
e150	108	12	9	22.06	110
e150 x 2	216	24	9	44.12	102
e150 x 4	432	48	9	86.75	108